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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,829	10/22/2001	Yong-Suk Go	8733.080.10	8486

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EXAMINER	
KOVALICK, VINCENT E	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,829	GO, YONG-SUK	
	Examiner	Art Unit	
	Vincent E Kovalick	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 25-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6 and 25-33* is/are allowed.

6)☒ Claim(s) *7,8 and 14* is/are rejected.

7)☒ Claim(s) *9-13 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Applicant's Reply to non-Final Officer Action dated July 8, 2004 in response to USPTO Office Action dated March 9, 2004.

In response to Applicant's remarks regarding the 35 U.S.C 112, first paragraph rejection of claim 25, Applicant's remarks have merit; the teaching of "n voltage converters" as described at page 7, line 30 - page 8, line 24 of the instant application is sufficient to overcome the rejection to claim 25, said rejection is herewith withdrawn.

Applicant's argument relative to claim 1 wherein the filing date of the Shau (USP 6,404,670) reference does not antedate the effective filing date of the subject matter currently claimed has merit, the rejection of claim 1 is herewith withdrawn.

Applicant's arguments regarding claim 7 have been fully considered but they are not persuasive. Applicant argues that Furuhashi et al. *inherently* discloses mean necessary for decompressing compressed data and for reconstructing signals suitable for presentation to a display requiring the multiple steps recited in col. 2, lines 39-44). One of ordinary skill in the art would not be limited in thinking that the method steps as taught by Furuhashi et al. is the only way to achieve this end. The teaching of Smeets provides another option for quantizing the analogue signal and assigning codeword.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the

time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Regarding claim 8, and the priority date of the Kondo reference, the feature of the 'analog signal level detecting circuit' is now taught in new Prior Art Koike (USP 4,244,259).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. (USP 5,850,540) taken with Smeets et al. (USP 6,218,968) in view of Taguchi (USP 5,815,080).

Relative to claims 7 and 14, Furuhashi et al. **teaches** a method and apparatus for timesharing CPU system bus in an image generation system (col. 3, lines 64-67; col. 3, lines 1-67; col. 4, lines 1-67 and col. 5, lines 1-53). Furuhashi et al. further **teaches** a bus decompressing apparatus compressing: receiving means for receiving an analog signal formed by compressing at least n-bit data, wherein n is an integer (col. 2, lines 46-54 and col. 3, lines 9-18 and 41-56). Furuhashi et al. **does not teach** quantizing means for quantizing the analog signal from the receiving means; and coding means connected to the quantizing means for coding the quantized analog signal to reconstruct the n-bit data; or a plurality of level detectors parallely connected to the input line to output a quantized signal.

Furuhashi et al. teaches receiving means for receiving a compressed analog signal.

Smeets et al. **teaches** a method for encoding data (col. col. 1, lines 42-67 and col. 2, lines 1-59).

Smeets et al. further **teaches** quantizing means for quantizing the analog signal from the receiving means; and coding means connected to the quantizing means for coding the quantized analog signal to reconstruct the n-bit data (col. 12, lines 41-44).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the devices of Furuhashi et al. the features as taught by Smeets et al in order to put in place the means necessary to decompress compressed data and reconstruct the signal being processed for presentation to a display device.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. taken with Smeets et al. as applied to claims 7 in item 9 hereinabove, and further in view of Koike (USP 4,244,259).

Relative to claims 8, Furuhashi et al. taken with Smeets et al. **does not teach** a bus decompressing apparatus wherein quantizing means includes at least (2 *to the* n *power* - 1) level detectors connected in parallel between the receiving means and the coding means, each level detector being configured to detect different voltage levels of the analog signal.

Furuhashi et al. taken with Smeets et al. teaches receiving means for receiving a compressed analog signal and quantizing means for quantizing the analog signal for further processing.

Koike **teaches** a voltage detection circuit (col. 5, lines 31-48). Koike further **teaches** quantizing means includes at least (2 *to the* n *power* - 1) level detectors connected in parallel between the receiving means and the coding means, each level detector being configured to detect different voltage levels of the analog signal (Abstract).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Furuhashi et al. taken with Smeets the feature as taught by

Koike in order to put in place the circuitry necessary to detect the various voltage levels associated with the compressed analog signal.

Allowable Subject Matter

5. Claims 9-13 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 9 the prior art of record **does not teach** a bus decompressing apparatus wherein each one of the level detectors comprises: a transistor controlled by the analog signal from the receiving means; and output voltage control means connected to the transistor to output the quantized analog signal to the coding means in response to the analog signal.

Regarding claim 13, the prior art of record **does not teach** a bus decompressing apparatus wherein the quantizing means includes first, second and third level detectors, each level detector having a transistor with a threshold voltage, the transistor being connected between a first voltage and a second voltage, wherein the transistor of the first level detector turns on when the analog signal is above the second voltage, the transistor of the second level detector turns on when the analog signal is above the second voltage by about 1/3 of the difference between the first and second voltages, and the transistor of the third level detector turns on when the analog signal is above the second voltage by about 2/3 of the difference between the first and second voltage.

6. Claims 1-6 and 25-33 are allowed.

7. The following is an examiner's statement of reasons for allowance:

Relative to claim 1, the major difference between the teachings of the prior art of record (Furuhashi et al.; Smeets et al. and Taguchi) and that of the instant invention is that said prior art of record **does not teach** a bus compressing apparatus comprising at least two voltage control

means connected to the corresponding bit lines, wherein each voltage control means changes the voltage level of the bit line at a different ratio from the other voltage control means.

Relative to claim 25, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a bus compressing apparatus for use in interfacing a controller and a display device for compressing n output signals of the controller, the bus compressing apparatus comprising: n voltage converters coupled to the corresponding output signals, wherein n is an integer and each voltage converter changes a voltage level of the corresponding output signal, and outputs of the n voltage converters are connected to produce a combined output signal in response to voltage levels of the n output signals from the controller, and wherein the combined output signal has a plurality of voltage levels representing nth power of the number of output signals.

Relative to claim 29, the major difference between the teachings of the prior art of record and that of the instant invention is that said prior art of record **does not teach** a bus decompressing apparatus comprising a coding device connected to a plurality of level detectors to code quantized signals to reconstruct an n-bit data.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,064,771	Migdal et al.
U. S. Patent No.	5,883,925	Sinibaldi et al.
U. S. Patent No.	4,951,139	Hamnilton et al.

Responses

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E Kovalick whose telephone number is 703 306-3020. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent E. Kovalick

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